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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Atty. Docket

ROLF GRZIBEK

PHD 98,014

Filed: CONCURRENTLY

Title: ARRANGEMENT FOR PROCESSING VIDEO SIGNALS

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please
amend the above-identified application as follows:

IN THE SPECIFICATION

Page 1, before line 1, insert the following heading:

--BACKGROUND OF THE INVENTION--;

before line 27, insert the following heading:

--SUMMARY OF THE INVENTION--;

Page 4, before line 18, insert the following heading:

--BRIEF DESCRIPTION OF THE DRAWINGS--;

line 18, delete "In the drawing:";

before line 25, insert the heading:

--DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS--.

IN THE ABSTRACT


Page 9, last line, delete "Fig. 1".

REMARKS

The specification has been amended to add headings in accordance with MPEP Section 601.

The above amendments are submitted to place the application in proper U.S. format. Early consideration and action on the merits are solicited.

Respectfully submitted,

By 
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Arrangement for processing video signals.

The invention relates to an arrangement for processing video signals provided as interlaced video signals generated in the interlaced scanning mode, in which two fields constitute one frame, and/or as pseudo-interlaced video signals derived from non-interlaced video signals obtained by means of progressive scanning.

5 State-of-the-art arrangements for processing video signals, for example, for mixing video signals are either implemented for video signals generated in accordance with the interlaced scanning mode or for video signals obtained by means of progressive scanning. Within an arrangement, a plurality of circuits may be provided, each one of which is, however, implemented either for video signals generated in the interlaced scanning mode or for video
10 signals obtained by means of progressive scanning. If such arrangements are to be suitable for both types of video signals, a considerable number of components will be required.

Video signals generated in the interlaced scanning mode are internationally denoted as "interlaced" signals. In such signals, two fields jointly constitute one frame. The fields are generated in such a way that they are temporally transmitted one after the other and,
15 upon display, are interlaced line by line in the interlaced scanning mode. The picture contents of the two fields may represent different motion phases of an object to be displayed. Video signals obtained by means of progressive scanning are internationally denoted as "non-interlaced" signals. In these signals, all picture lines of a frame are generated in a continuous consecutive sequence. Interlaced fields are then obtained.

20 It is known to convert non-interlaced video signals into such video signals in which a frame originally scanned in accordance with this scanning mode is split up into two fields. These are actually not fields, as are present in interlaced video signals, but a split-up non-interlaced frame. These frames are hereinafter denoted as pseudo-interlaced, because they can be transmitted similarly as fields of interlaced video signals in electronic arrangements.
25 However, it should be noted that such fields of a pseudo-interlaced video signal must be processed in the same way.

It is an object of the invention to provide an arrangement for processing video signals of the type described in the opening paragraph, which, with a minimal number of

components, allows both interlaced video signals and non-interlaced or pseudo-interlaced video signals to be processed.

According to the invention, this object is achieved in that at least one video signal-processing unit is provided which receives at least an interlaced video signal or at least a pseudo-interlaced video signal and processes these video signals in dependence upon control data generated by means of a control unit, and in that a clock generator is provided which controls the control unit and/or the video signal-processing unit in such a way that, when processing an interlaced video signal or a pseudo-interlaced video signal, possibly new control data are generated and/or taken into account as from the start of its next field or its next frame, respectively.

The video signal-processing unit processes the video signals. This unit may receive either a conventional interlaced video signal or a pseudo-interlaced video signal which is obtained by splitting up the frames of non-interlaced video signals into two pseudo-fields.

Two fields of a frame of an interlaced video signal can be processed in different ways. For example, the two fields may be subjected to a continuously changing mixing process because the two fields are displayed temporally one after the other. For a non-interlaced or pseudo-interlaced video signal, this is, however, not appropriate because the two generated pseudo-fields of a pseudo-interlaced video signal belong to a frame and display the same motion phase of the picture contents. If the two pseudo-fields were processed in different ways, this would be noticeable as interference in the picture upon the display of the non-interlaced video signal.

According to the invention, the control unit controlling the video signal processing by means of control data is controlled by means of a clock generator in such a way that fields of an interlaced video signal and pseudo-fields of a pseudo-interlaced video signal are processed in different ways.

When an interlaced video signal is processed, the clock generator controls the control unit or the video signal-processing unit in such a way that possibly changed control data are generated at the start of every new field or are taken into account by the video signal-processing unit. This means that at the start of every new field, the processing mode of the fields may be changed. As explained above, this is allowable for fields of an interlaced video signal.

However, if a pseudo-interlaced video signal is processed by the video signal-processing unit, then this is not allowable. In this case, the clock generator controls the control unit and the video signal-processing unit in such a way that only from the start of a new frame,

i.e. the first pseudo-field of a frame, a new, changed mode of processing is performed by the video signal-processing unit. It is thereby ensured that two consecutive pseudo-fields of a pseudo-interlaced video signal belonging to the same frame of a non-interlaced video signal are processed in the same way so that no picture interferences become visible within this frame.

This arrangement is thus capable of processing both interlaced video signals and pseudo-interlaced video signals obtained from non-interlaced video signals. Dependent on the type of video signal, the control unit or the video signal-processing unit is controlled in such a way that optimal processing, adapted to the type of the video signal, takes place. In this way, only one video signal-processing unit is required for both types of video signals.

For an embodiment of the invention as claimed in claim 2, a buffer memory is provided which takes over the control data supplied by the control unit. The video signal-processing unit itself takes over the control data directly from the buffer memory and processes the video signals in dependence upon these control data. In this case, the video signal-processing unit may be implemented in such a way that it immediately takes a change of the control data into account, independently of the fact which field is processed next.

To ensure the different ways of processing the two types of video signals as explained above, the buffer memory is controlled by the clock generator in such a way that new control data can be taken over by the buffer memory at the start of every new field when an interlaced video signal is being processed. When a pseudo-interlaced video signal is being processed, the buffer memory is, however, controlled by means of the clock generator in such a way that new control data possibly generated by the control unit are taken over by the buffer memory only at the start of the next frame, i.e. the first pseudo-field of a pseudo-interlaced video signal.

Alternatively to the solution as claimed in claim 2, a further embodiment of the invention as claimed in claim 3 is characterized in that the control unit is already implemented in such a way that it supplies data at the appropriate times only. In this case, the buffer memory mentioned above is not required but may still be provided for practical reasons.

In accordance with a further embodiment as claimed in claim 4, the information about the fact which field of a video signal to be processed is present can be advantageously supplied to the clock generator by means of an externally generated genlock signal which is provided anyway in professional video-processing arrangements.

In accordance with a further embodiment as claimed in claim 5, the signal-processing unit may also be used advantageously for mixing a plurality of video signals.

It may be desirable to further process processed non-interlaced video signals and processed interlaced video signals separately, because these signals are to be further transmitted, for example, via different transmission paths. For this case, an embodiment as claimed in claim 6 provides at least two video signal-processing units, each of which process only allocated video signals which can be further processed separately. In this way, for example, pictures generated for a broadcast may be processed parallel in an interlaced or non-interlaced format. The two signal sequences may be processed in the same way so that the pictures are subjected to the same processors.

If a non-interlaced video signal to be processed is not already present in a pseudo-interlaced form, the conversion means as claimed in claim 7 are suitable for converting this video signal into the pseudo-interlaced format. Conversely, the reconversion means as claimed in claim 8 may be advantageously used for reconverting a pseudo-interlaced video signal processed in the arrangement into a non-interlaced video signal.

These and other aspects of the invention are apparent from and will be elucidated with reference to the embodiments described hereinafter.

In the drawing:

Fig. 1 is a block diagram of a first embodiment of the arrangement for processing video signals according to the invention, in which a buffer memory controlled by a clock generator is provided, and

Fig. 2 is a block diagram of a second embodiment of the arrangement according to the invention, in which the clock generator controls a control unit of the video signal-processing unit.

The block diagram, shown in Fig. 1, of the first embodiment of the video signal processing arrangement shows a video signal-processing unit 1. The video signal-processing unit 1 is used for processing video signals applied thereto, for example, for mixing or changing them in another way.

The video signal-processing unit 1 processes video signals in dependence upon control data which are generated by means of a control unit 2. The control unit 2 supplies these control data to a buffer memory 3. The video signal-processing unit 1 takes over the control data in a temporally undelayed manner from the buffer memory 3 and processes the video signals in a mode dependent on these control data. This is possibly effected without any

noticeable delay, i.e. when control data change, the processing of the video signals changes accordingly.

The buffer memory 3 is controlled by means of a clock generator 4 which receives an externally generated genlock signal. The clock generator 4 controls the buffer memory in such a way that new control data are only taken over by this buffer memory when this is desirable in dependence upon the video signal. For example, when an interlaced video signal is being processed, possibly new control data are taken over by the buffer memory every time at the start of a new field. However, when a pseudo-interlaced video signal is processed, the buffer memory is controlled by the clock generator 4 in such a way that new control data are only taken over at the start of a new frame, i.e. at the start of the first pseudo-field of a pseudo-interlaced video signal.

It is thereby achieved that, in the case of non-interlaced video signals or pseudo-interlaced video signals, the processing is changed only at the start of a new frame so that all pseudo-fields of the pseudo-interlaced video signal are processed in the same way.

A non-interlaced video signal may be directly applied to the video signal-processing unit 1. Also a non-interlaced video signal converted already into the pseudo-interlaced form may be directly applied to this unit. A non-interlaced video signal, which is still present in its original form and is obtained by means of progressive scanning, is converted into a pseudo-interlaced video signal by optionally provided conversion means 5. A frame of such a non-interlaced video signal is then split up into two pseudo-fields which can be processed in a similar manner as the fields of a non-interlaced video signal. However, it should be noted for such pseudo-fields that they are to be processed in the same way.

Dependent on the type of signals processed by the video signal-processing unit 1, these signals are supplied in the same form again. If processed pseudo-interlaced video signals should be converted into non-interlaced video signals again, reconversion means 6 are optionally provided, which perform this conversion.

A second embodiment of the arrangement according to the invention, also shown in the form of a block diagram in Fig. 2, corresponds to the first embodiment shown in Fig. 1, but the buffer memory 3 is not provided. Moreover, the clock generator 4 directly controls the control unit 2.

In this embodiment, the control unit 2 is controlled by the clock generator 4 in such a way that, when an interlaced video signal is being processed, it supplies new, modified control data only at the start of every new field and, when a pseudo-interlaced video signal is being processed, only at the start of a new frame, i.e. at the start of the first pseudo-field of a

pseudo-interlaced video signal. In this way, it is also ensured that new, modified control data through the video signal-processing unit 1 are only taken into account at the desired instants.

The two embodiments of the arrangement according to the invention ensure that two pseudo-fields of a frame of a pseudo-interlaced video signal are processed in the same way. If this signal is reconverted into a conventional non-interlaced video signal, it is ensured that all picture lines of the frame are processed in the same way. This is important because these lines of a frame display identical motion phases. However, when a non-interlaced video signal is being processed, two fields of a frame may be processed in different ways, if desired, because they are displayed temporally one after the other and represent different motion phases. This differentiation in the processing of the video signals is obtained by means of the arrangement according to the invention with a small number of components. Moreover, such an arrangement can be very flexibly used for different types of video signals.

CLAIMS:

1. An arrangement for processing video signals provided as interlaced video signals generated in the interlaced scanning mode, in which two fields constitute one frame, and/or as pseudo-interlaced video signals derived from non-interlaced video signals obtained by means of progressive scanning, characterized in that at least one video signal-processing unit (1) is provided which receives at least an interlaced video signal or at least a pseudo-interlaced video signal and processes these video signals in dependence upon control data generated by means of a control unit (2), and in that a clock generator (4) is provided which controls the control unit (2) and/or the video signal-processing unit (1) in such a way that, when processing an interlaced video signal or a pseudo-interlaced video signal, possibly new control data are generated and/or taken into account as from the start of its next field or its next frame, respectively.
2. An arrangement as claimed in claim 1, characterized in that a buffer memory (3) is provided for the control data, from which buffer memory the video signal-processing unit (1) directly takes over and employs the control data and which is controlled by the clock generator (4) in such a way that it takes over new control data when processing an interlaced video signal or a pseudo-interlaced video signal at the start of its next field or its next frame, respectively.
3. An arrangement as claimed in claim 1, characterized in that the clock generator (4) controls the control unit (2) in such a way that it supplies new control data to the video signal-processing unit when processing an interlaced video signal or a pseudo-interlaced video signal at the start of its next field or its next frame, respectively.
4. An arrangement as claimed in claim 1, characterized in that the clock generator (4) is controlled by means of a genlock signal which comprises information about the synchronizing signals of the video signal to be processed.

5. An arrangement as claimed in claim 1, characterized in that the video signal-processing unit (1) is provided to mix at least two video signals.

6. An arrangement as claimed in claim 1, characterized in that two video signal-processing units (1) are provided, a first of which is provided to process one or more interlaced video signals and a second is provided to process one or more pseudo-interlaced video signals.

7. An arrangement as claimed in claim 1, characterized in that conversion means (5) are provided to convert non-interlaced video signals into pseudo-interlaced video signals having a scanning line and sync pulse structure which is similar to that of interlaced signals and allows said signals to be processed in the video signal-processing unit.

8. An arrangement as claimed in claim 1, characterized in that reversion means (6) are provided which convert pseudo-interlaced signals supplied by the video signal-processing unit into non-interlaced video signals and supply them as such.

ABSTRACT:

In an arrangement for processing video signals provided as interlaced video signals generated in the interlaced scanning mode, in which two fields constitute one frame, and/or as pseudo-interlaced video signals derived from non-interlaced video signals obtained by means of progressive scanning, flexible use of the arrangement with a minimal number of components for this arrangement is achieved in that at least one video signal-processing unit (1) is provided which receives at least an interlaced video signal or at least a pseudo-interlaced video signal and processes these video signals in dependence upon control data generated by means of a control unit (2), and in that a clock generator (4) is provided which controls the control unit (2) and/or the video signal-processing unit (1) in such a way that, when processing an interlaced video signal or a pseudo-interlaced video signal, possibly new control data are generated and/or taken into account as from the start of its next field or its next frame, respectively.

Fig. 1

1/1

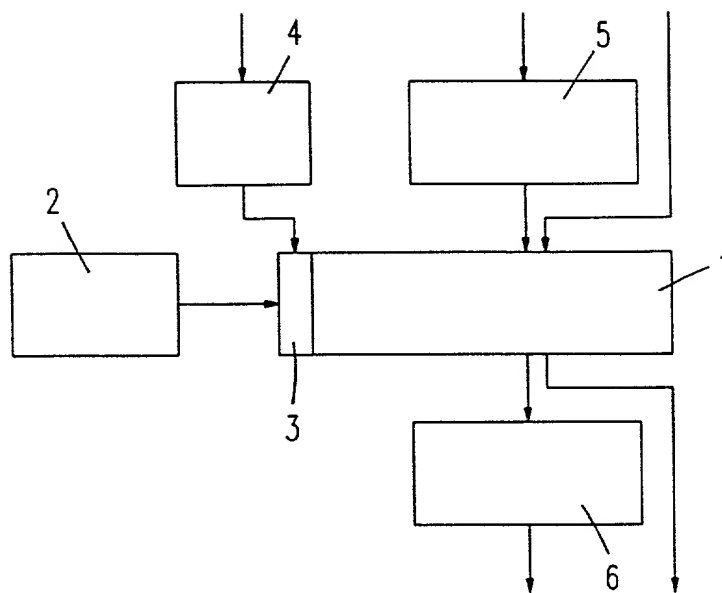


Fig.1

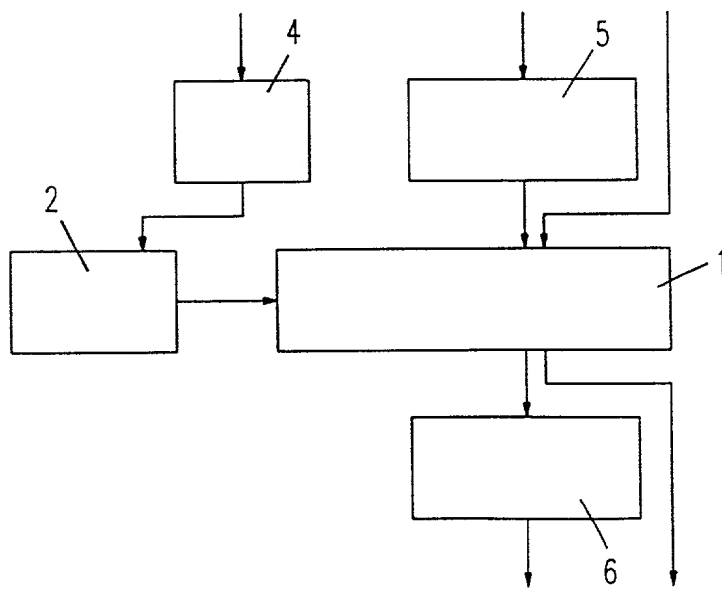


Fig.2

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ROLF GRZIBEK

PHD 98,014

Filed: CONCURRENTLY

Title: ARRANGEMENT FOR PROCESSING VIDEO SIGNALS

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

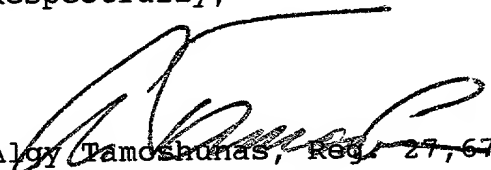
GREGORY L. THORNE

(Registration No. 39,398)

c/o U.S. PHILIPS CORPORATION, Intellectual Property
Department, 580 White Plains Road, Tarrytown, New York
10591, his Associate Attorney(s)/Agent(s) with all the usual
powers to prosecute the above-identified application and any
division or continuation thereof, to make alterations and
amendments therein, and to transact all business in the
Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND
THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE
UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,


Alvy Tamoshunas, Reg. 27,677
Attorney of Record

Dated at Tarrytown, New York
on February 8, 1999.

DECLARATION and POWER OF ATTORNEY

ATTORNEY'S DOCKET NO.:
PHD 98.014

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"Arrangement for processing video signals"**

the specification of which (check one)

☐ is attached hereto.

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APP.NUMBER	DATE OF FILING (DATE,MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Germany	19808005.0	26 February 1998	YES

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Algy Tamoshunas, Reg. No. 27,677
Jack E. Haken, Reg. No. 26,902

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